IDEC Chip Design Contest

A Semi-Digital Charge-Domain CDC with Configurable Subtraction for Wide-Range, High-Resolution Sensing

Jisu Kim[1)], Taeho Lee[2)], and Jun-Eun Park[1)]
[1)]Department of Electrical and Computer Engineering, [2)]Department of Semiconductor Convergence Engineering, Sungkyunkwan University, Suwon, Republic of Korea

Abstract

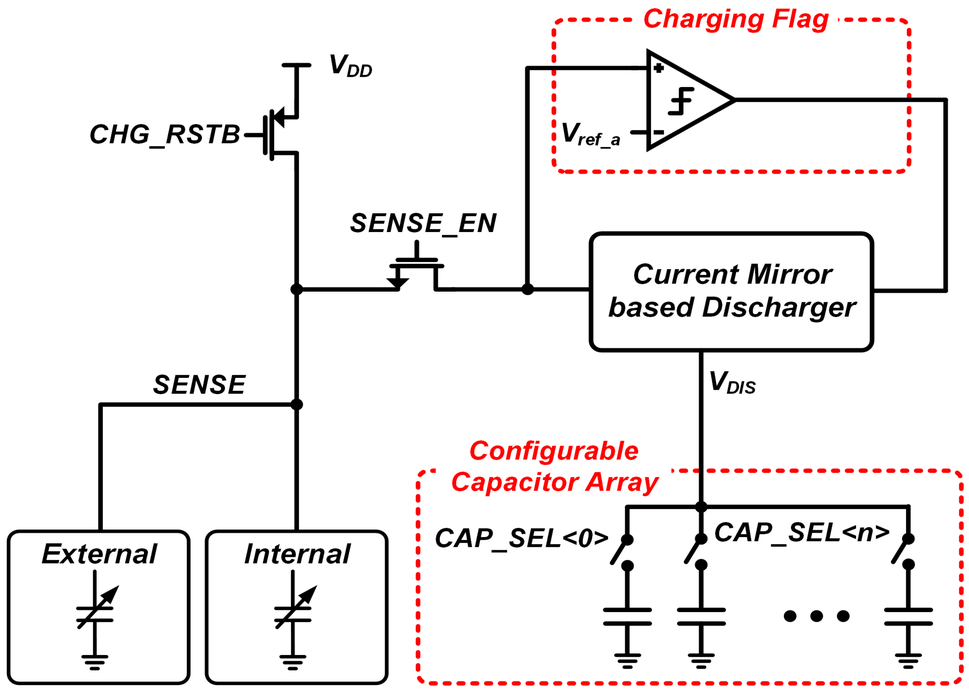
A semi-digital capacitance-to-digital converter (CDC) supporting up to 1 nF input range using a configurable charge subtraction capacitor and a current mirror-based discharger. The single-slope discharge technique enables energy-efficient operation without complex analog blocks like OTAs. The design achieves high resolution and low power , offering flexibility for various sensing applications. Post-layout simulation confirms 10 fF resolution with stable performance.

Proposed Design

• **The proposed CDC** is based on **a self-sensing mechanism,** allowing the selection between an external sensing capacitor or an internal capacitor.

• **Current mirror-based discharger** with a charging flag enables **repetitive, accurate capacitance measurement** by resetting and recharging the sensor capacitor each cycle based on a reference voltage comparison

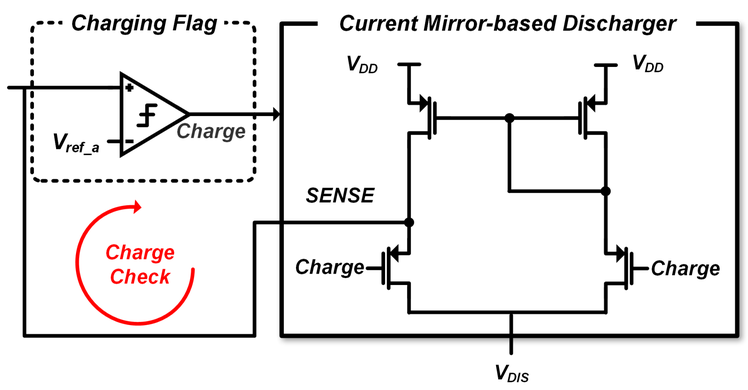
• **Configurable subtraction capacitor array** enables **flexible adjustment of input range and resolution**, allowing accurate digital conversion of sensor capacitance through discharge cycle counting.



Current Mirror-based Discharger

• **The current mirror-based discharger** uses a comparator to monitor the sense node voltage and triggers a charging flag when it fall below a reference level, resetting the discharge process.

• **Current mirror-based discharger** enables repetitive charge-discharge cycles, allowing accurate digital conversion of sensor capacitance while supporting a wide input range.

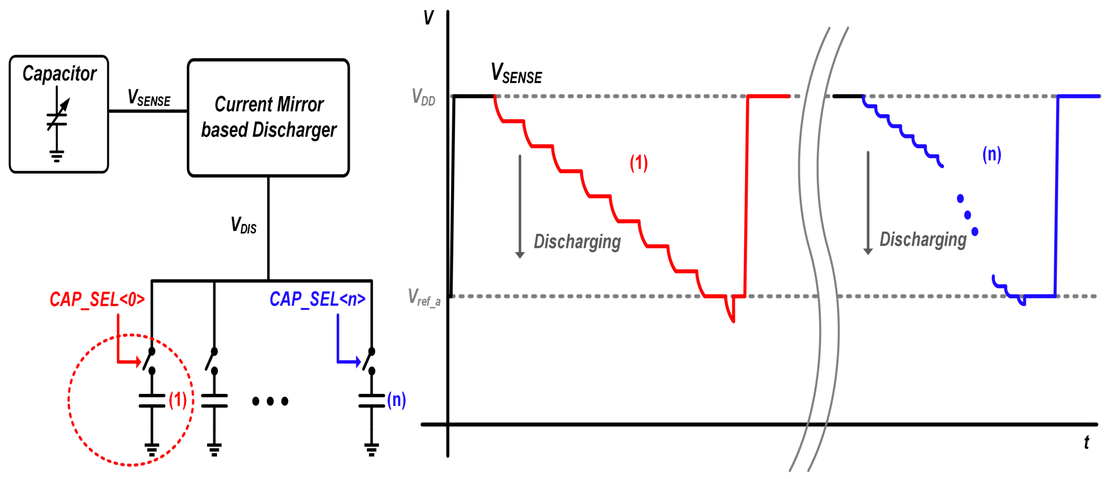


Configurable Capacitor Array

• **Configurable subtraction capacitor array** allows dynamic selection of discharge capacitor based on application needs, enabling flexibility in input capacitance range and resolution.

• By **adjusting the subtraction capacitor size**, the number of discharge cycles and voltage step size can be controlled, influencing both measurement speed and accuracy.

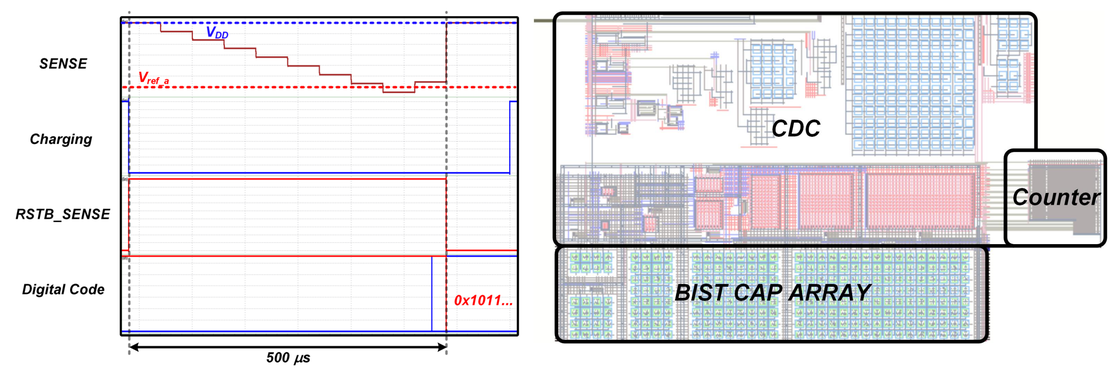
• This architecture supports **a wider range of sensor capacitances** and is especially suitable for adaptable, **high-resolution sensing applications.**



Simulations Results

• Simulation results show that the proposed CDC accurately converts capacitances up to 1 nF within 500 μs, maintaining a consistent minimum resolution of 10 fF across various ranges.

• Increasing the subtraction capacitor reduces conversion time and discharge cycles, while enabling a broader measurable capacitance range with low power consumption of 135.72 μW.



Conclusions

The proposed CDC employs a semi-digital architecture with a configurable subtraction capacitor and current mirror-based discharger, enabling accurate and energy-efficient conversion over a wide input range up to 1 nF. It eliminates the need for OTAs, reducing complexity, and achieves 10 fF resolution, validating its suitability for high-precision capacitive sensing applications.

Reference

W. Jung. et al. “27.6 A 0.7 pF-to 10 nF Fully Digital Capacitance-to-Digital Converter Using Iterative Delay-Chain Discharge”, International Solid-State Circuits Conference, pp. 484-486, 2015.